19-5841; Rev 0; 5/11

EVALUATION KIT AVAILABLE

MAX9599

Low-Power Programmable Gamma Buffers

General Description

The MAX9599 provides multiple programmable reference voltages for gamma correction in TFT LCDs. Each gamma output comprises a 10-bit digital-to-analog converter (DAC) and high current buffer, which reduces the recovery time of the output voltages when critical levels and patterns are displayed. A precision-programmable internal reference sets the full-scale voltage of the DACs.

The IC contains nonvolatile multiple-time-programmable (MTP) memory to store the reference data and all of the gamma output codes.

The gamma output voltages, the programmable reference, and the nonvolatile memory are all programmed digitally through the 1MHz (fast mode plus) I²C interface.

Applications

Notebook and Tablet TFT LCDs

Monitors

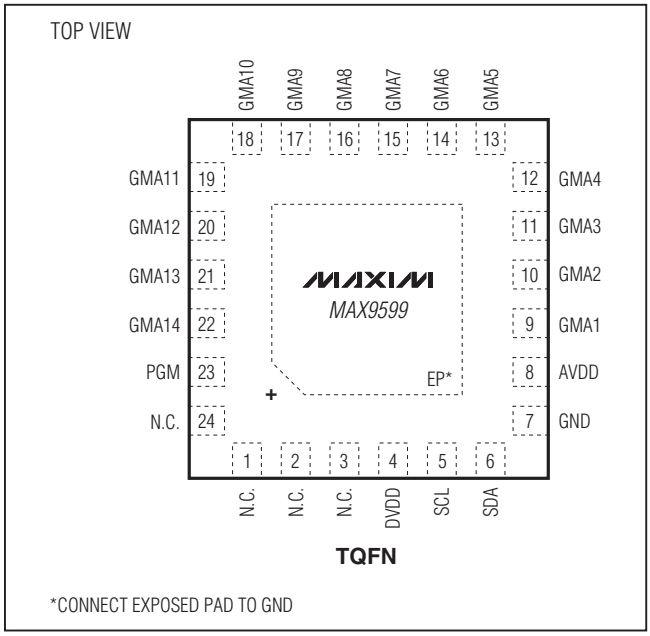
Features

- **28mW Quiescent Power**
- **4mm x 4mm Package**
- **14-Channel, 10-Bit Programmable Gamma**
- **Nonvolatile MTP Memory (300x Rewrite)**

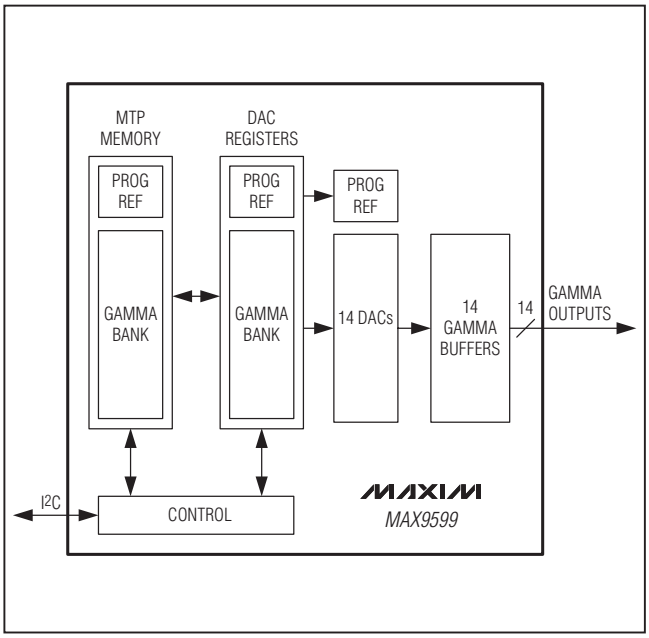
***Ordering Information* appears at end of data sheet.**

*For related parts and recommended products to use with this part, refer to **www.maxim-ic.com/MAX9599.related**.*

Pin Configuration



Simplified Block Diagram



***Note:** Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, go to: **www.maxim-ic.com/errata**.*

ABSOLUTE MAXIMUM RATINGS

(All voltages are with respect to GND.)
Supply Voltages
AVDD .....-0.3V to +12V
DVDD .....-0.3V to +6V
PGM .....-0.3V to +36V
Outputs
GMA1–GMA14 ..... -0.3V to (V_{AVDD} + 0.3V)
Inputs
SDA, SCL .....-0.3V to +6V
Continuous Current
SDA, SCL ..... ±20mA
GMA1–GMA14 ..... ±50mA

Continuous Power Dissipation (T_A = +70°C)
24-Pin TQFN Multilayer Board
(derate 27.8mW/°C above +70°C).....2222.2mW
Junction Temperature .....+125°C
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) .....+260°C

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN
Juction-to-Ambient Thermal Resistance (θ_{JA}) .....36°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....3°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = 8V, V_{DVDD} = 2.5V, V_{PGM} = 24V, V_{GND} = 0V, programmable reference code = 800, no load, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLIES						
AVDD Analog Supply Voltage Range	V_{AVDD1}	Guaranteed by PSRR	7		11	V
Digital Supply Voltage	V_{DVDD}		2.25		5.5	V
AVDD Analog Quiescent Current	I_{AVDD}			3	4	mA
Digital Quiescent Current	I_{DVDD}	No SCL or SDA transitions		1.5	2.1	mA
PGM Program Supply Voltage Range	V_{PGM}	Required when programming MTP memory only	18		33	V
PGM Supply Current	I_{PGM}	When programming MTP memory		5		mA
		Normal operation		5	16	µA
Thermal Shutdown				160		°C
Thermal Shutdown Hysteresis				15		°C
DVDD Undervoltage Lockout Threshold	UVLO_D			1.8		V

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = 8V, V_{DVDD} = 2.5V, V_{PGM} = 24V, V_{GND} = 0V, programmable reference code = 800, no load, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PROGRAMMABLE REFERENCE (V_{PREF})						
Full-Scale Voltage		Referred to output, T_A = +25°C	9.99	10	10.01	V
		T_A = -40°C to +85°C	9.98	10	10.02	
Resolution			10			Bits
Integral Nonlinearity Error		T_A = +25°C, 16 ≤ reference code ≤ 1008		0.7	1.5	LSB
Differential Nonlinearity Error		T_A = +25°C, 16 ≤ reference code ≤ 1008		0.5	1	LSB
DAC						
Resolution			10			Bits
Integral Nonlinearity Error		T_A = +25°C, 16 ≤ code ≤ 1008		0.5	1	LSB
Differential Nonlinearity Error		T_A = +25°C, 16 ≤ code ≤ 1008		0.5	1	LSB
GAMMA OUTPUTS						
Short-Circuit Current		Output connected to either supply rail		50		mA
Total Output Error		T_A = +25°C, code = 768		2		mV
Load Regulation		-5mA ≤ I_{LOAD} ≤ +5mA, code = 768		0.5		mV/mA
Low Output Voltage		Sinking 2mA, referred to lower supply rail		0.15	0.2	V
High Output Voltage		Sourcing 2mA, referred to upper supply rail	-0.25	-0.15		V
Power-Supply Rejection Ratio		Code = 768, V_{AVDD} = 7V to 11V	60	90		dB
		Code = 768, frequency = 120kHz		34		
Output Resistance		Buffer is disabled		154		kΩ
Maximum Capacitive Load		Placed directly at output		100		pF
Settling Time		Settling to 0.5 LSB, C_{LOAD} = 50pF, 0 to 15mA load step		2		µs
Noise		RMS noise (10MHz bandwidth)		375		µV
MTP MEMORY						
Maximum Writes to Each Register				300		Times
MTP Write Time		Per 10-bit register programmed		35		ms
MTP Transfer Time		Time to transfer all data to DAC registers		400		µs

Note 2: 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.

DIGITAL I/O CHARACTERISTICS

(V_{DVDD} = 2.5V, V_{GND} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		0.7 x V_{DVDD}			V
Input Low Voltage	V_{IL}				0.3 x V_{DVDD}	V
Hysteresis of Schmitt Trigger Inputs	V_{HYS}		0.05 x V_{DVDD}			V
Low-Level Output Voltage	V_{OL}	Open drain, I_{SINK} = 3mA	0		0.4	V
Low-Level Output Current	I_{OL}	V_{OL} = 0.4V	20			mA
Input Leakage Current	I_{IH}, I_{IL}	V_{IN} = 0V or DVDD	-10	+0.01	10	µA
Input Capacitance				5		pF
Power-Down Input Current	I_{IN}	V_{DVDD} = 0V, V_{IN} = 1.98V	-10		+10	µA

I²C TIMING CHARACTERISTICS

(V_{DVDD} = 2.5V, V_{GND} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

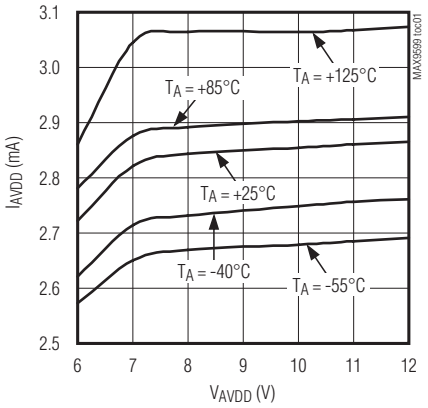
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial-Clock Frequency	f_{SCL}		0		1000	kHz
Hold Time (REPEATED) START Condition	$t_{HD,STA}$	After this period, the first clock pulse is generated	0.26			µs
SCL Pulse-Width Low	t_{LOW}		0.5			µs
SCL Pulse-Width High	t_{HIGH}		0.26			µs
Setup Time for a REPEATED START Condition	$t_{SU,STA}$		0.26			µs
Data Hold Time	$t_{HD,DAT}$	I²C bus devices	0			ns
Data Setup Time	$t_{SU,DAT}$		50			ns
SDA and SCL Receiving Rise Time	t_R				120	ns
SDA and SCL Receiving Fall Time	t_F				120	ns
SDA Transmitting Fall Time	t_F				140	ns
Setup Time for STOP Condition	$t_{SU,STO}$		0.26			µs
Bus Free Time Between STOP and START Conditions	t_{BUF}		0.5			µs
Bus Capacitance	C_B				550	pF
Data Valid Time	$t_{VD;DAT}$				0.45	µs
Data Valid Acknowledge Time	$t_{VD;ACK}$				0.45	µs
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns

Low-Power Programmable Gamma Buffers

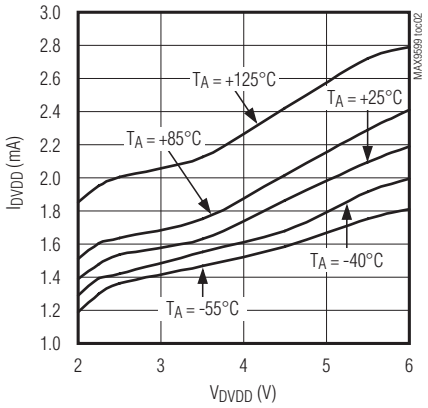
Typical Operating Characteristics

(V_{AVDD} = 8V, V_{DVDD} = 2.5V, V_{GND} = 0V, Programmable Reference Code = 800, no load, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

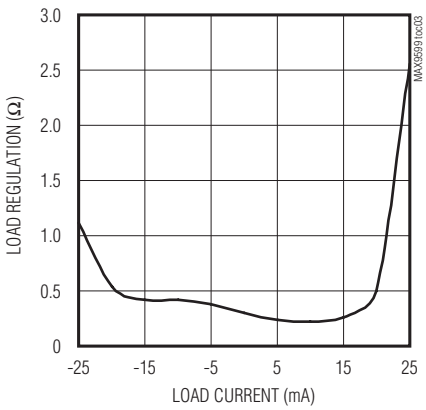
AVDD SUPPLY CURRENT vs. AVDD SUPPLY VOLTAGE



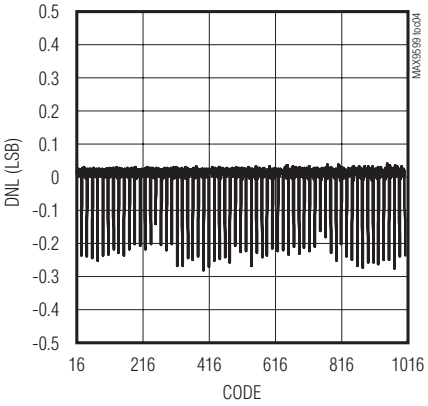
DVDD SUPPLY CURRENT vs. DVDD SUPPLY VOLTAGE



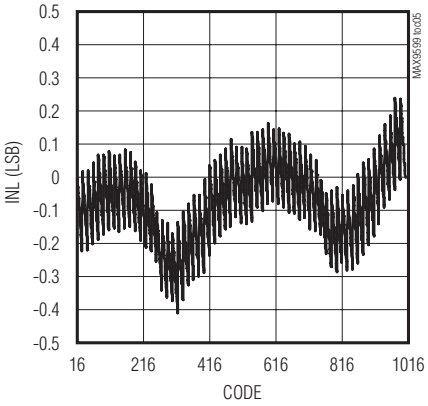
GAMMA OUTPUT LOAD REGULATION



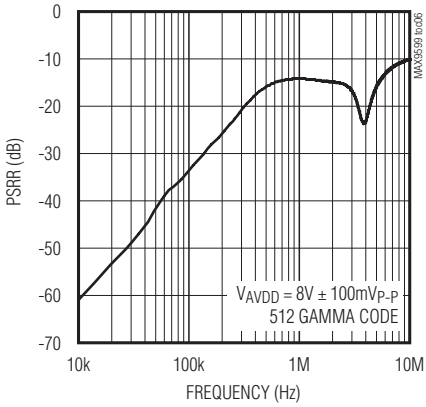
GAMMA DNL



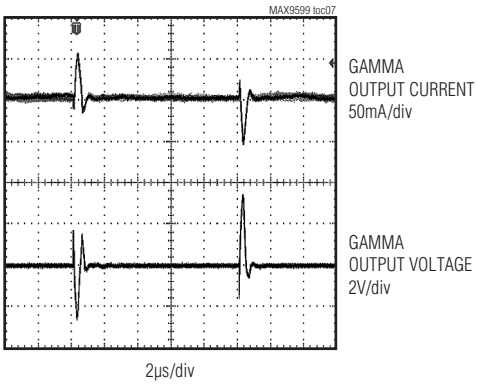
GAMMA INL



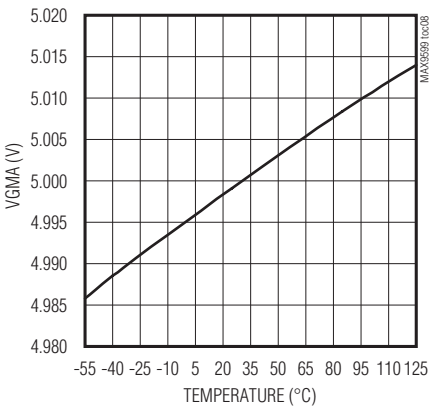
POWER-SUPPLY REJECTION RATIO (GAMMA)



GAMMA OUTPUT LOAD TRANSIENT



GAMMA OUTPUT vs. TEMPERATURE

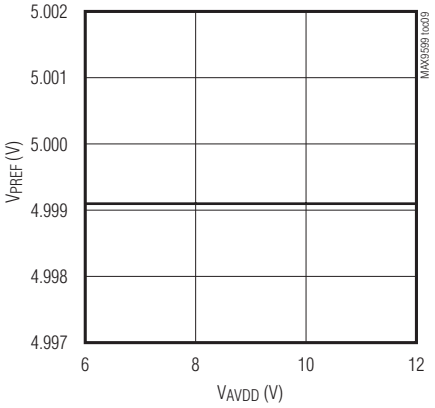


Low-Power Programmable Gamma Buffers

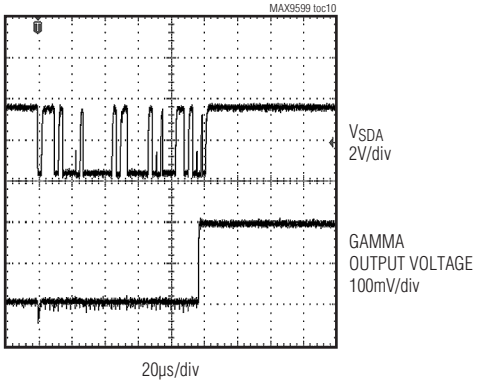
Typical Operating Characteristics (continued)

(V_{AVDD} = 8V, V_{DVDD} = 2.5V, V_{GND} = 0V, Programmable Reference Code = 800, no load, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

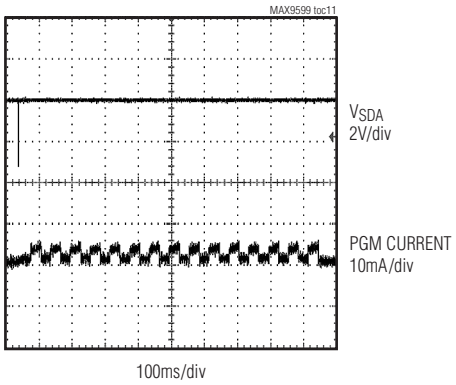
GAMMA OUTPUT vs. AVDD VOLTAGE



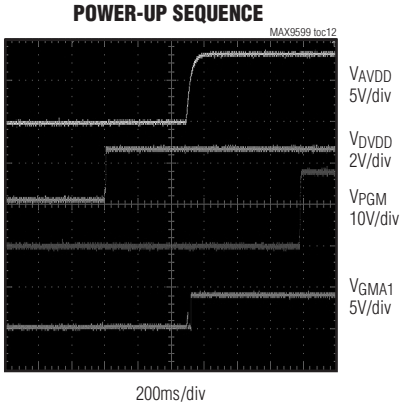
GAMMA PROGRAM TO OUTPUT DELAY



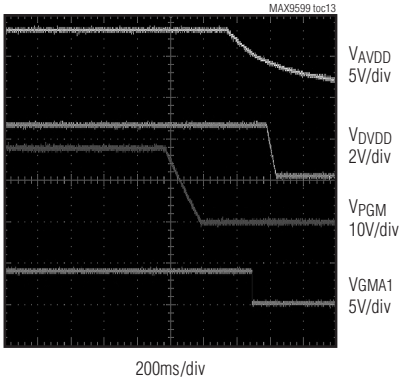
PGM CURRENT DURING MTP BURNING



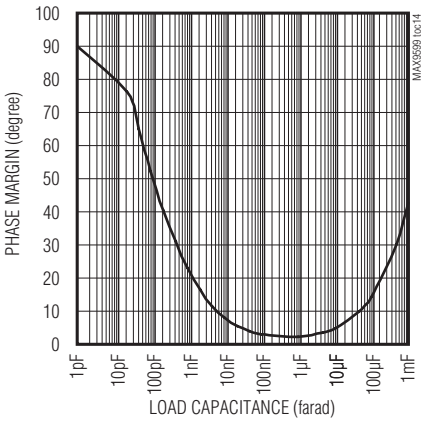
POWER-UP SEQUENCE



POWER-DOWN SEQUENCE

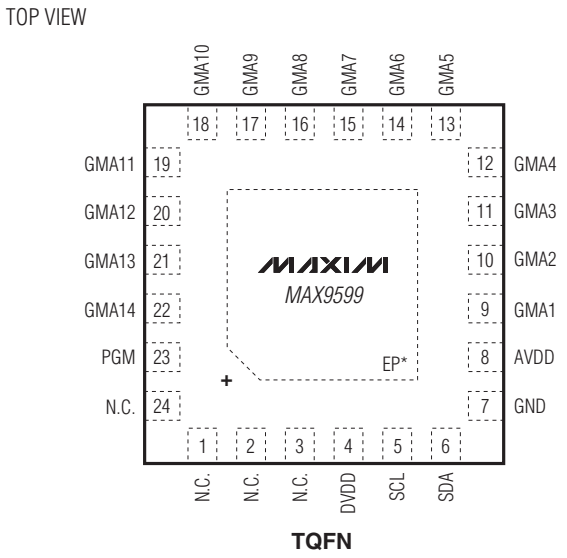


PHASE MARGIN vs. LOAD CAPACITANCE



Low-Power Programmable Gamma Buffers

Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1, 2, 3, 24	N.C.	No Internal Connection
4	DVDD	Digital Power Supply. Bypass DVDD with a 0.1µF capacitor to GND.
5	SCL	I²C-Compatible Serial-Clock Input
6	SDA	I²C-Compatible Serial-Data Input/Output
7	GND	Ground Pin. Must be connected to board GND.
8	AVDD	Analog Power Supply. Bypass AVDD with a 0.1µF capacitor to GND.
9	GMA1	Gamma DAC Analog Output 1
10	GMA2	Gamma DAC Analog Output 2
11	GMA3	Gamma DAC Analog Output 3
12	GMA4	Gamma DAC Analog Output 4
13	GMA5	Gamma DAC Analog Output 5
14	GMA6	Gamma DAC Analog Output 6
15	GMA7	Gamma DAC Analog Output 7
16	GMA8	Gamma DAC Analog Output 8
17	GMA9	Gamma DAC Analog Output 9

Pin Description (continued)

PIN	NAME	FUNCTION
18	GMA10	Gamma DAC Analog Output 10
19	GMA11	Gamma DAC Analog Output 11
20	GMA12	Gamma DAC Analog Output 12
21	GMA13	Gamma DAC Analog Output 13
22	GMA14	Gamma DAC Analog Output 14
23	PGM	Program Supply Voltage Pin. Required for programming MTP memory only. Requires typically 5mA current when programming MTP memory.
—	EP	Exposed Pad. EP must be connected to board GND.

Detailed Description

The MAX9599 contains 14 channels of 10-bit fully-programmable gamma DACs and buffers. The transient response of the gamma output buffers is fast, eliminating display issues caused by source driver charge injection and other transients. In addition, the gamma output buffers are capable of driving large capacitive loads.

The MAX9599 integrates a programmable reference voltage (V_{PREF}) for the DACs, eliminating the need for an external reference voltage. Accuracy of the full-scale programmable reference voltage is ±0.1%, and resolution is 10 bits. The programmable reference voltage has very high DC and AC power-supply rejection.

Programmable Reference

The MAX9599 has an internal programmable reference which, when referred to the output, has a full-scale voltage of 10V (±0.1%). The reference voltage is calculated using the following equation:

$$V_{PREF} = (10V \times CODE)/1024$$

where CODE is the numeric value stored in the internal register (0 to 1023). Note that V_{PREF} cannot reach 10V because the maximum value of CODE is 1023, not 1024.

The value of PREF is independent of the AVDD supply voltage because the PREF block is low-voltage internally, so voltage headroom is not an issue. For example, with an AVDD supply of 8V, PREF can be set up to 10V; the actual gamma output voltages are limited by AVDD since the gamma buffers have AVDD as the positive supply.

10-Bit Digital-to-Analog Converters

V_{PREF} sets the full-scale output of the DACs. Determine the output voltages using the following equations:

$$V_{GMA\_} = (V_{PREF} \times CODE)/1024$$

where CODE is the numeric value of the DAC's binary input code (0 to 1023).

Note that the DAC can never output V_{PREF} because the maximum value of CODE is always one LSB less than the reference.

Gamma Buffers

The source drivers can kick back a great deal of current to the buffer outputs during a horizontal line change or a polarity switch. The DAC output buffers can source/sink 50mA of peak transient current to reduce the recovery time of the output voltages when critical levels and patterns are displayed.

Multiple-Time Programmable (MTP) Nonvolatile Memory

The IC contains nonvolatile memory for storing the gamma and reference values on-chip. Each register can be rewritten up to 300 times. Writing to MTP memory requires all three supply pins (AVDD, DVDD, and PGM) to be above their minimum voltages; any MTP write commands issued will be ignored otherwise.

To read from MTP requires only the DVDD supply. On power-up, once the DVDD is above the minimum voltages, the MTP memory values are automatically transferred to the DAC registers.

Program Pin (PGM)

The IC has a program pin that requires a high voltage for MTP memory programming only. When programming MTP memory, the PGM pin must be above its minimum voltage for the entire duration of the programming, and the supply should be capable of sourcing up to 20mA. When not programming MTP memory, the PGM pin sinks very little current, and the voltage on the pin does not matter.

Power-On Reset (POR)/Power-Up

The IC contains an integrated POR circuit that ensures all registers are reset to a known state on power-up. Once DVDD rises above its UVLO threshold, the POR circuit releases the registers for normal operation. Should the internal supply input drop to less than the threshold, the contents of the IC registers can no longer be guaranteed. After power-up or a POR event, the outputs (GMA1 through GMA14) are in high-impedance mode until the gamma data from the MTP memory is finished transferring to the DAC registers.

Column Driver Protection

During power-up and before valid data is written to the registers, the IC operates in a safe mode to protect the column drivers. While in this mode, the 14 gamma outputs remain in high impedance. The output buffers are enabled once valid data is written to all the I²C registers from the MTP memory.

SMBus is a trademark of Intel Corp.

Thermal Shutdown

The IC features thermal-shutdown protection with temperature hysteresis. When the die temperature reaches +165°C, all of the gamma outputs are disabled (high-impedance). When the die cools down by 15°C, the outputs are enabled again.

I²C Serial Interface

The IC features an I²C/SMBus™-compatible, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). Figure 1 shows the 2-wire interface timing diagram.

Pullup Resistors and Input Protection

A pullup resistor with a value greater than 500Ω is required between SDA and DVDD. SCL operates as only an input. A pullup resistor with a value greater than 500Ω is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the devices from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

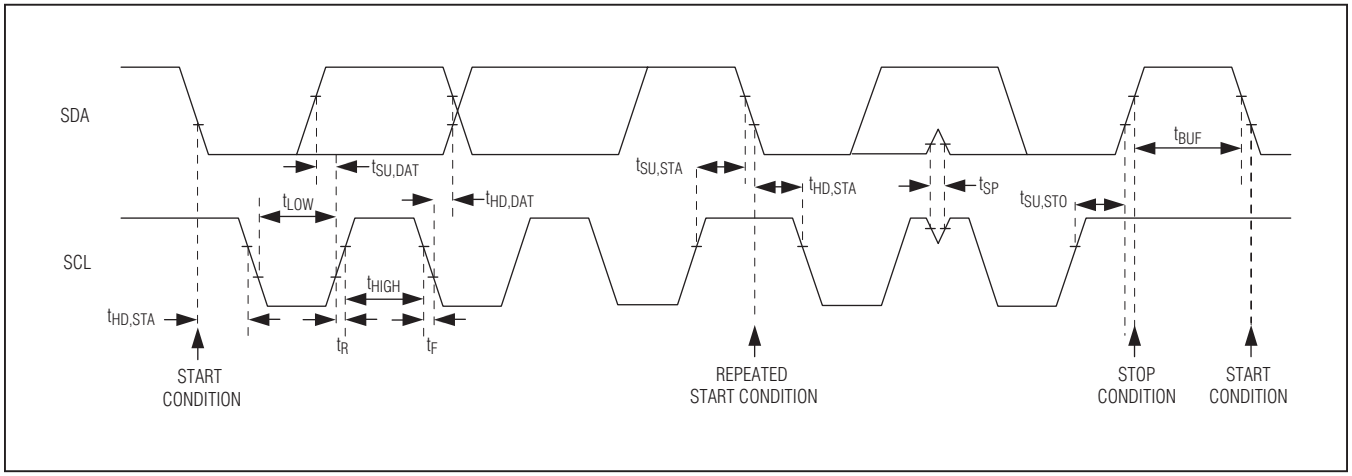


Figure 1. I²C Interface Timing Diagram

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals. See the *START and STOP Conditions* section. SDA and SCL idle high when the I²C bus is not in use.

START and STOP Conditions

A master initiates communication by issuing a START (S) condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP (P) condition is a low-to-high transition on SDA while SCL is high. A START condition from the master signals the beginning of a transmission to the IC. The master terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START (Sr) condition is generated instead of a STOP condition.

Early STOP Conditions

The IC recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the IC uses to handshake receipt of each byte of data when in write mode (Figure 3). The IC pulls down SDA during the entire master-generated ninth clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master may retry communication.

The master pulls down SDA during the ninth clock cycle to acknowledge receipt of data when the IC is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not acknowledge (NACK) is sent when the master reads the final byte of data from the IC, followed by a STOP condition.

Slave Address

The slave address is defined as the 7 most significant bits (MSBs) followed by the read/write (R/W) bit. Set the R/W bit to 1 to configure the IC to read mode. Set the R/W bit to 0 to configure the IC to write mode. The address is the first byte of information sent to the IC after the START condition. The IC's slave address is set internally. Table 1 shows the possible addresses for the IC.

Table 1. Slave Addresses for the IC

READ ADDRESS	WRITE ADDRESS
E9h (11101001)	E8h (11101000)

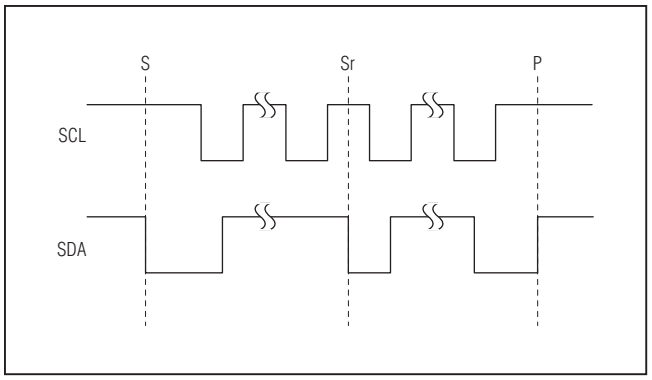


Figure 2. START, STOP, and REPEATED START Conditions

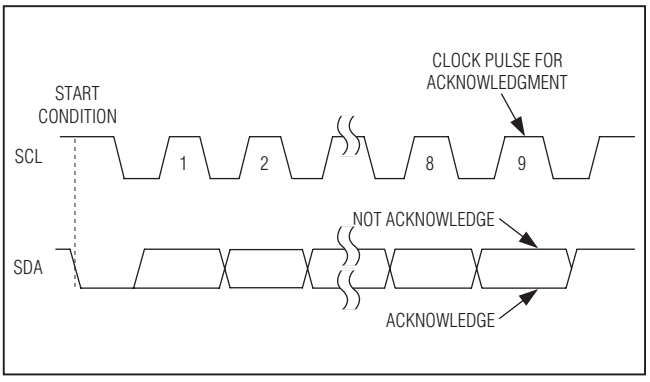


Figure 3. Acknowledge

10-Bit Register Structure

The IC has a 10-bit register, which requires two data bytes (16 bits) to be read or written in each transaction. Only the 10 least significant bits (LSBs) are written to the registers (Table 2). During a write operation, the write control bits (the two MSBs) are stripped from the incoming data stream and are used to determine whether the MTP or DAC registers are updated (Table 3).

Writing Data to the IC

Write Control Bits

The write control bits are utilized as they are received, so they should only be set on the final data word sent in the write transaction. Data received after a word with the write control bits set to 01 or 10 are ignored, and a new I²C transaction is necessary to write more data.

Write Command Format

A write to the IC comprises a START condition, the slave address (with the R/W bit set to 0), one data byte to configure the internal register address pointer, one word (two bytes) of data or more, and a STOP condition. Figure 4 illustrates the proper frame format for writing one word of data to the IC. Figure 5 illustrates the frame format for writing multiple words of data to the IC.

As shown in the figures, the register addresses occupy the 6 LSBs of the address byte. The two memory transfer bits (M1 and M0) are used for transferring data from the MTP to DAC registers and should be set to 0b00 when writing data. The pointer tells the IC where to write the next byte of data. An acknowledge pulse is sent by the IC upon receipt of the address pointer data when writing to the DAC registers. When writing to the MTP, a not acknowledge is sent from the IC after the master writes the final byte of data, followed by a STOP condition.

The third and fourth bytes sent to the IC contain the data to be written, along with the two write control bits. The address pointer autoincrements to the next register address after receiving every 16-bit data word (two bytes). This autoincrement feature allows the user to write all of the IC registers within one continuous frame.

Table 2. Data Register Structure

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
W1	W0	X	X	X	X	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0

Note: *The 10 LSBs contain the 10-bit data, and the 2 MSBs contain write control bits that determine whether the DAC registers or MTP registers are updated.*

Table 3. Write Control Bits

W1	W0	ACTION
0	0	No update.
0	1	MTP register(s) are updated when the current 16-bit data word is received. See the *Multiple-Time Programmable (MTP) Nonvolatile Memory* section for more details.
1	0	DAC register(s) are updated when the current 16-bit data word is received.
1	1	No update.

Note: *These two bits accompany every 10-bit write command. The MTP register(s) or DAC register(s) are updated as soon as a 16-bit data word is received with these bits set to 0b01 or 0b10.*

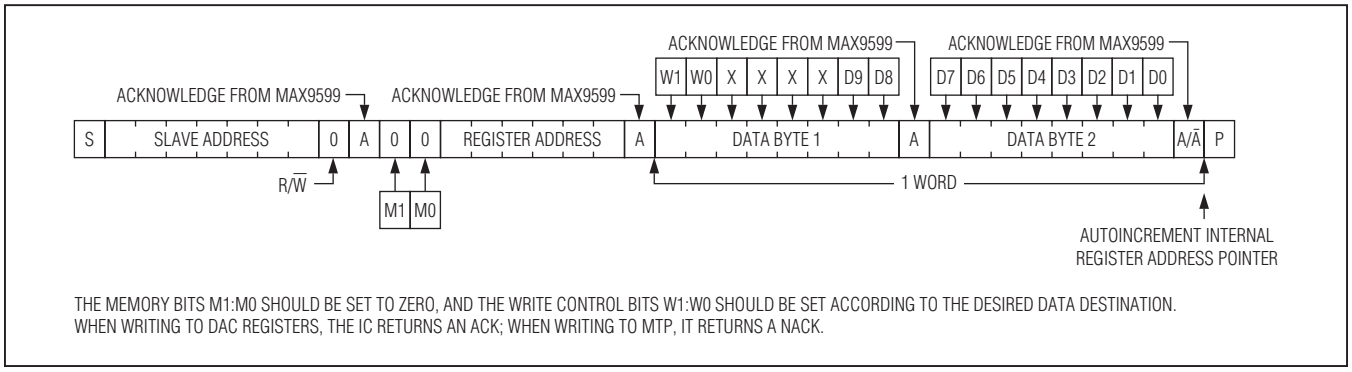


Figure 4. Writing a Word of Data to the IC's DAC or MTP Registers

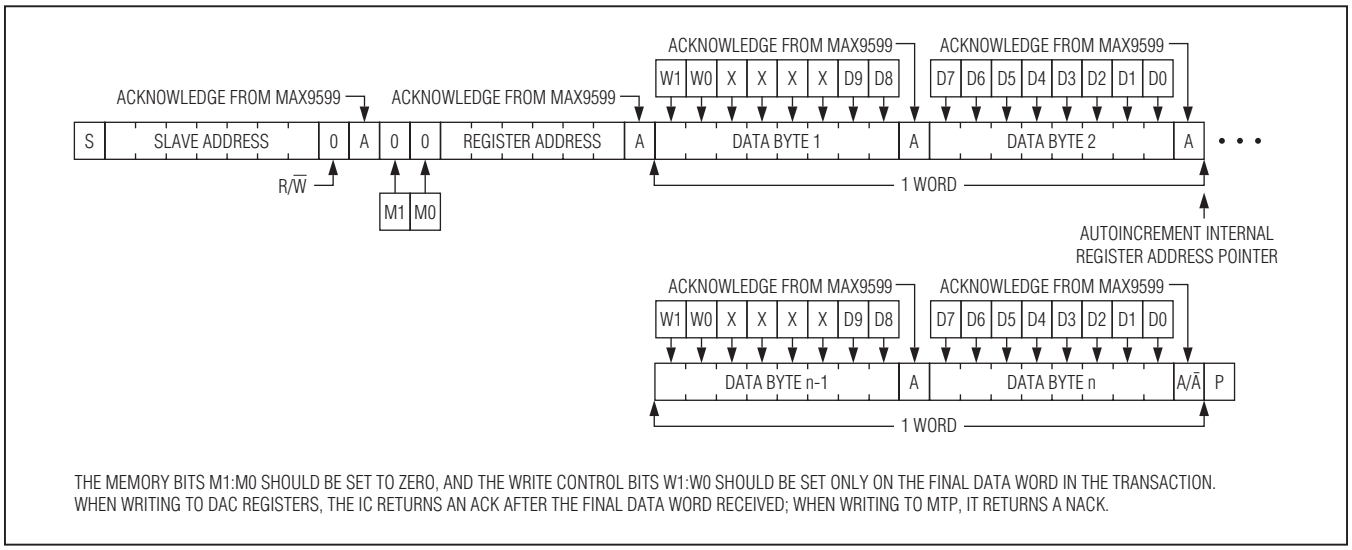


Figure 5. Writing Multiple Words of Data to the IC's DAC or MTP Registers

Writing to MTP Memory

Programming the MTP registers automatically updates the DAC registers and output voltages with the same codes. All the outputs are programmed and updated simultaneously. However, depending on the number of MTP registers, it takes up to 430ms to store the values into MTP memory. During this time, the IC is not available on the I²C bus and any communication from the master should be delayed until the MTP is programmed. Any attempt from the I²C master to talk to the IC is not acknowledged.

Reading Data from the IC

Read Data Format

Reading data from the IC requires the master to preset the address pointer by issuing a write command (slave address with R/W bit set to 0), followed by the desired register address. A REPEATED START condition should then be sent, followed by a read command (slave address with the R/W bit set to 1). The IC then transmits data, starting with the contents of the specified register. The address pointer autoincrements after every data word sent (2 bytes). This autoincrement feature allows all registers to be read sequentially within one continuous frame.

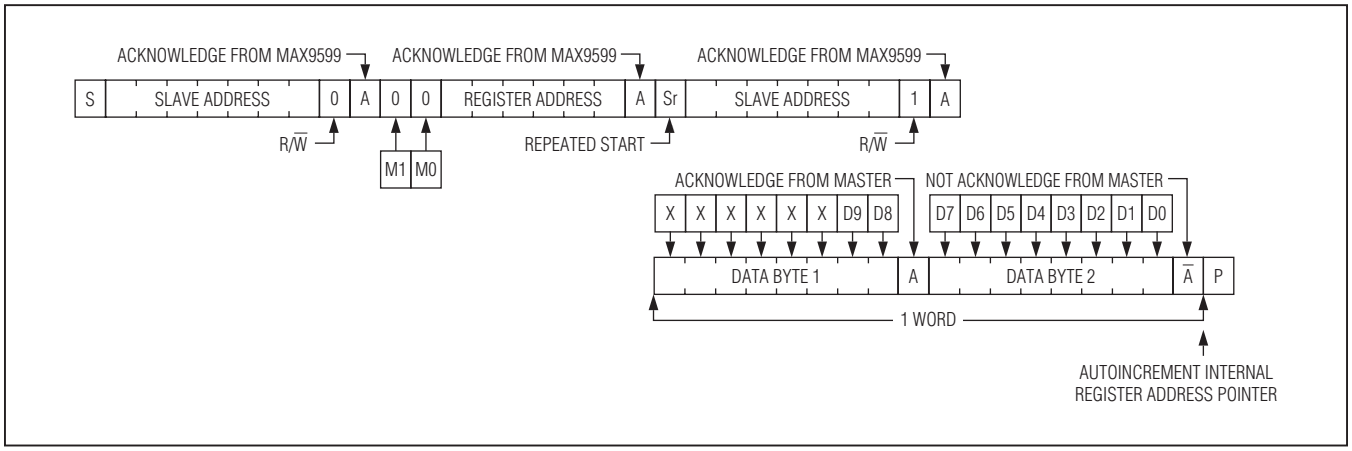


Figure 6. Reading One Word of Data from the IC

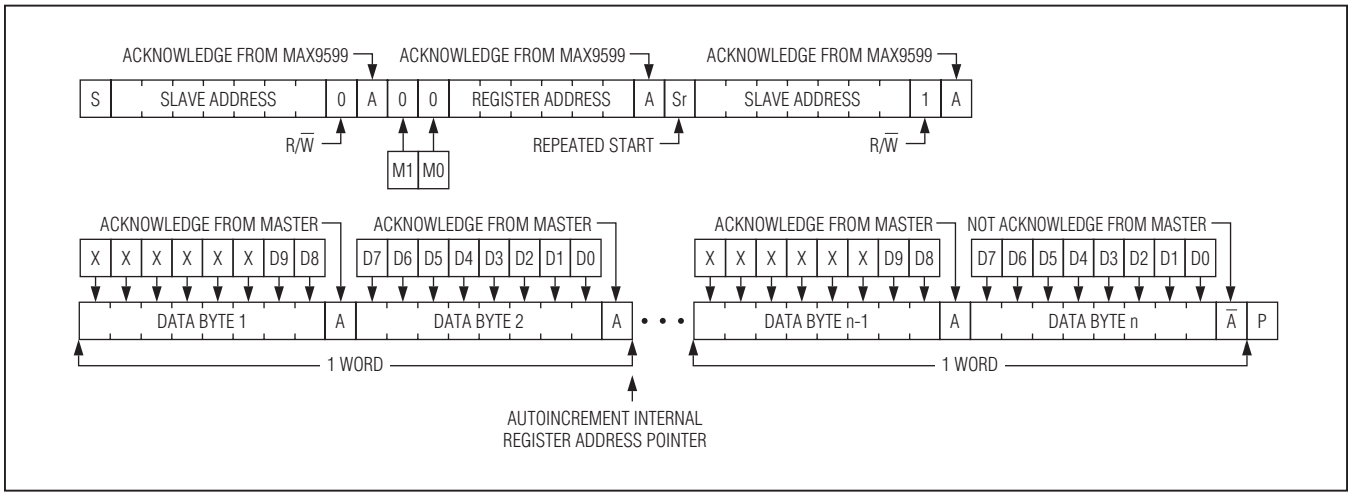


Figure 7. Reading Multiple Words of Data from the IC

A STOP condition can be issued after any number of read data bytes. The STOP condition does not reset the address pointer, so subsequent reads picks up where the previous one left off.

The I²C master must acknowledge all received data bytes except for the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. Figures 6 and 7 illustrate the frame format for reading data from the IC.

Reading Data from MTP Memory

To read the data in the MTP memory, it is necessary to first transfer the memory data into the DAC registers, then read the DAC registers as described in this section. See the section on *Updating the DAC Outputs from MTP Memory* for more information.

Updating the DAC Outputs from MTP Memory

It is possible to transfer the code to a single DAC register from the corresponding MTP register, or update all DAC registers at once. The process involves setting the memory transfer bits, the two MSB bits sent with the I²C register address. See Figures 8 and 9 for a graphical description of the single or general memory acquire commands.

Memory Transfer Bits

Table 4 shows the memory transfer bits used to set this function. These two bits are sent along with the I²C register address byte as part of a standard read or write command.

Register and Bit Descriptions

Table 5 shows the register map for the IC, including the factory-default values programmed into the MTP memory. Each register address points to a 10-bit register of data that must be read and written using two full bytes through the I²C interface. The least significant byte (LSB) holds the bottom 8 bits of the 10-bit data, while the most significant byte (MSB) holds the top 2 bits, as shown in Table 2.

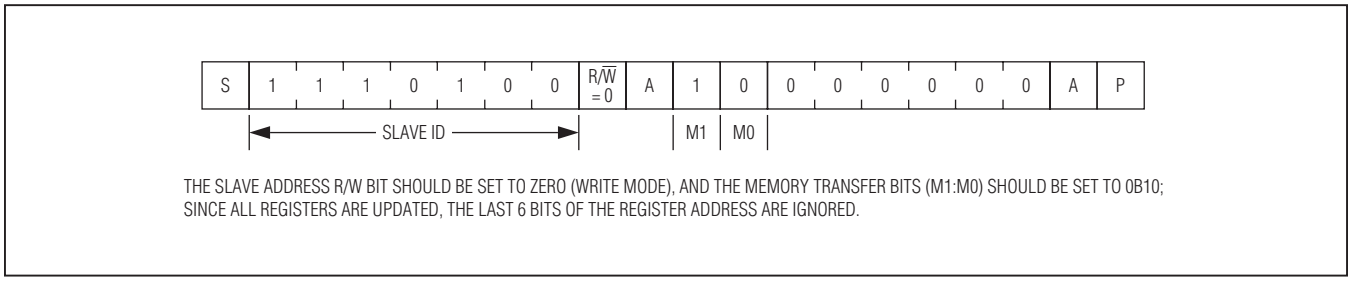


Figure 8. Updating All DAC Registers from MTP Memory Data (General Acquire Command)

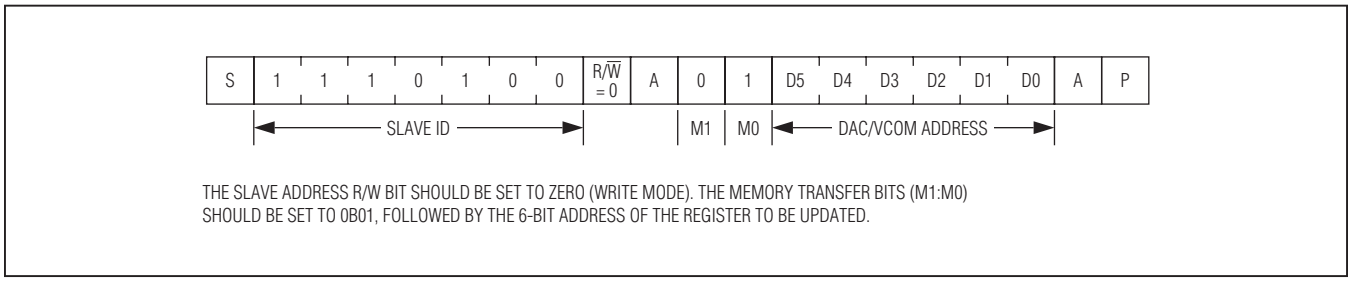


Figure 9. Updating a Single DAC Register with MTP Memory Data (Single Acquire Command)

Table 4. MTP Memory Transfer Bits

M1	M0	ACTION
0	0	No MTP transfer.
0	1	Only the addressed DAC register is set to the corresponding MTP value.
1	0	All I²C registers and DAC registers are set to their corresponding MTP values.
1	1	No MTP transfer.

Table 5. Detailed Description of the IC's 10-Bit DAC and MTP Memory Registers

REGISTER ADDRESS	REGISTER NAME	REGISTER DESCRIPTION	READ/WRITE?	MTP MEMORY DEFAULT VALUE
0x00	PREF	Programmable voltage reference	Read and write	0x0333
0x01	GMA1	Gamma 1	Read and write	0x03BC
0x02	GMA2	Gamma 2	Read and write	0x0377
0x03	GMA3	Gamma 3	Read and write	0x0333
0x04	GMA4	Gamma 4	Read and write	0x02EF
0x05	GMA5	Gamma 5	Read and write	0x02AB
0x06	GMA6	Gamma 6	Read and write	0x0266
0x07	GMA7	Gamma 7	Read and write	0x0222
0x08	GMA8	Gamma 8	Read and write	0x01DE
0x09	GMA9	Gamma 9	Read and write	0x019A
0x0A	GMA10	Gamma 10	Read and write	0x0155
0x0B	GMA11	Gamma 11	Read and write	0x0111
0x0C	GMA12	Gamma 12	Read and write	0x00CD
0x0D	GMA13	Gamma 13	Read and write	0x0089
0x0E	GMA14	Gamma 14	Read and write	0x0044

Applications Information

Power Sequencing

The AVDD and DVDD supply pins are independent of each other, and can be powered up and powered down in any sequence without damage to the IC. The sequence in Figure 10 is recommended to ensure that the analog outputs are always in a known state.

On power-up, the MTP memory is transferred into the DAC registers as soon as AVDD and DVDD are both above their undervoltage lockout (UVLO) voltages. Once the PGM output is also brought up, the MTP memory can be programmed.

PCB Layout and Grounding

If the IC is mounted using reflow soldering or waver soldering, the ground vias for the exposed pad should have a finished hole size of at least 14 mils to ensure adequate wicking of soldering onto the exposed pad. If the IC is mounted using solder mask technique, the vias requirement does not apply. In either case, the exposed pad on the TQFN package is electrically connected to both digital and analog grounds through a low thermal resistance path to ensure adequate heat dissipation. Do not route traces under these packages. The layout of the exposed pad should have multiple small vias over a single large via as shown as Figure 11. Thermal resistance between top and ground layers can be optimized with multiple small vias, and it is recommended to have plated via with 15 mils diameter. The vias should be flooded with solder for good thermal performance.

Power-Supply Bypassing

The IC operates from a single analog supply (AVDD) and a single digital supply (DVDD). Bypass AVDD to GND with 0.1µF and 10µF capacitors in parallel. Use an extensive ground plane to ensure optimum performance. Bypass DVDD and PGM to GND with 0.1µF capacitors. The 0.1µF bypass capacitors should be as close as possible to the IC and appropriately rated to handle the voltages. Refer to the MAX9599 Evaluation Kit for a proven PCB layout.

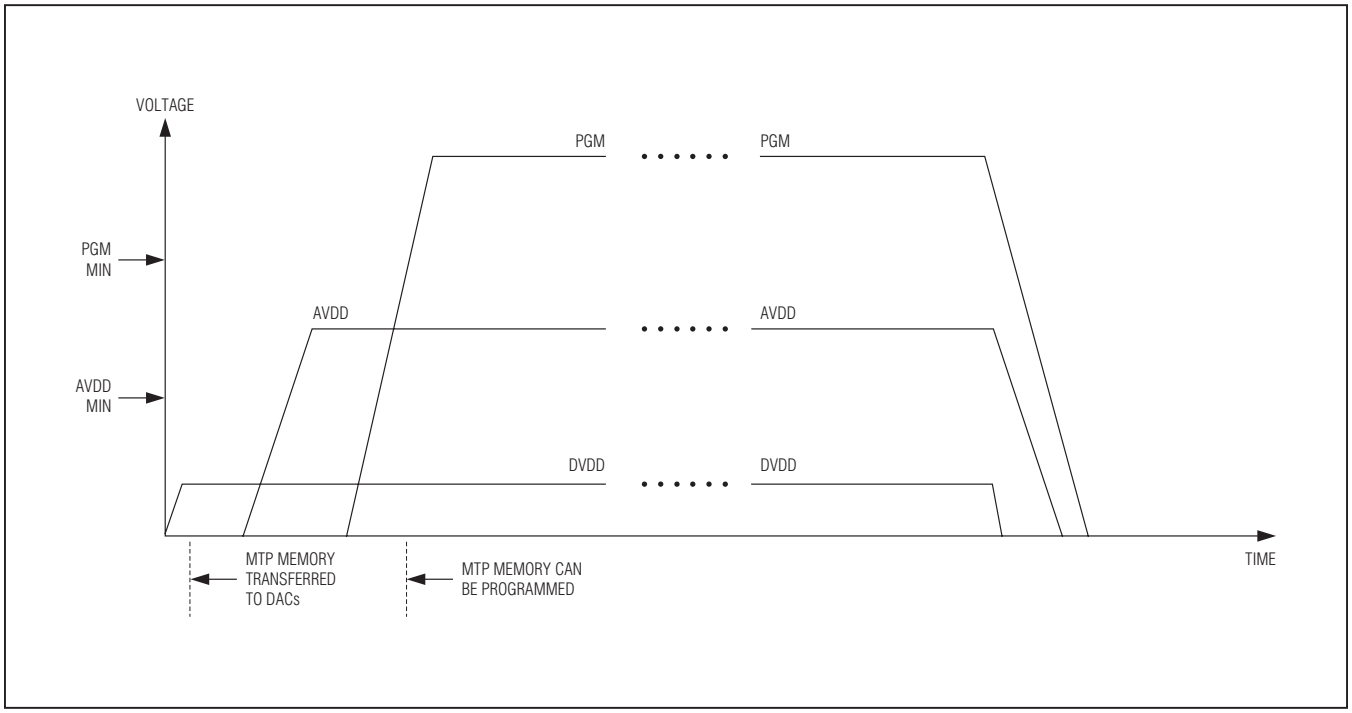


Figure 10. Conventional Power-Up and Power-Down Sequence

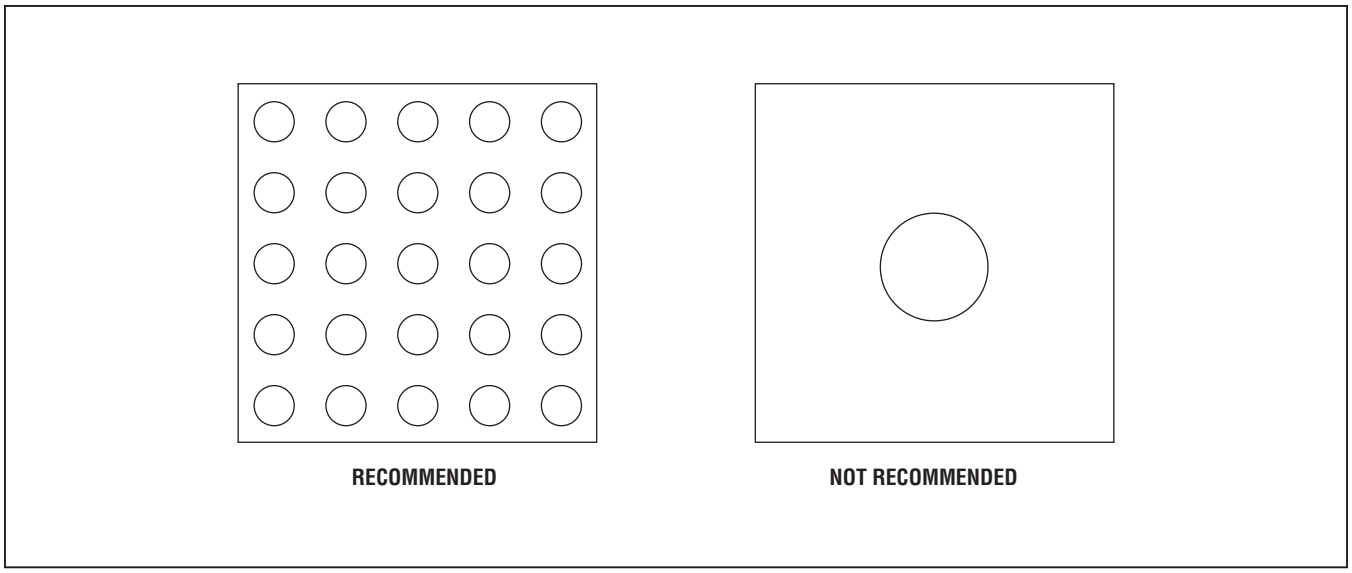
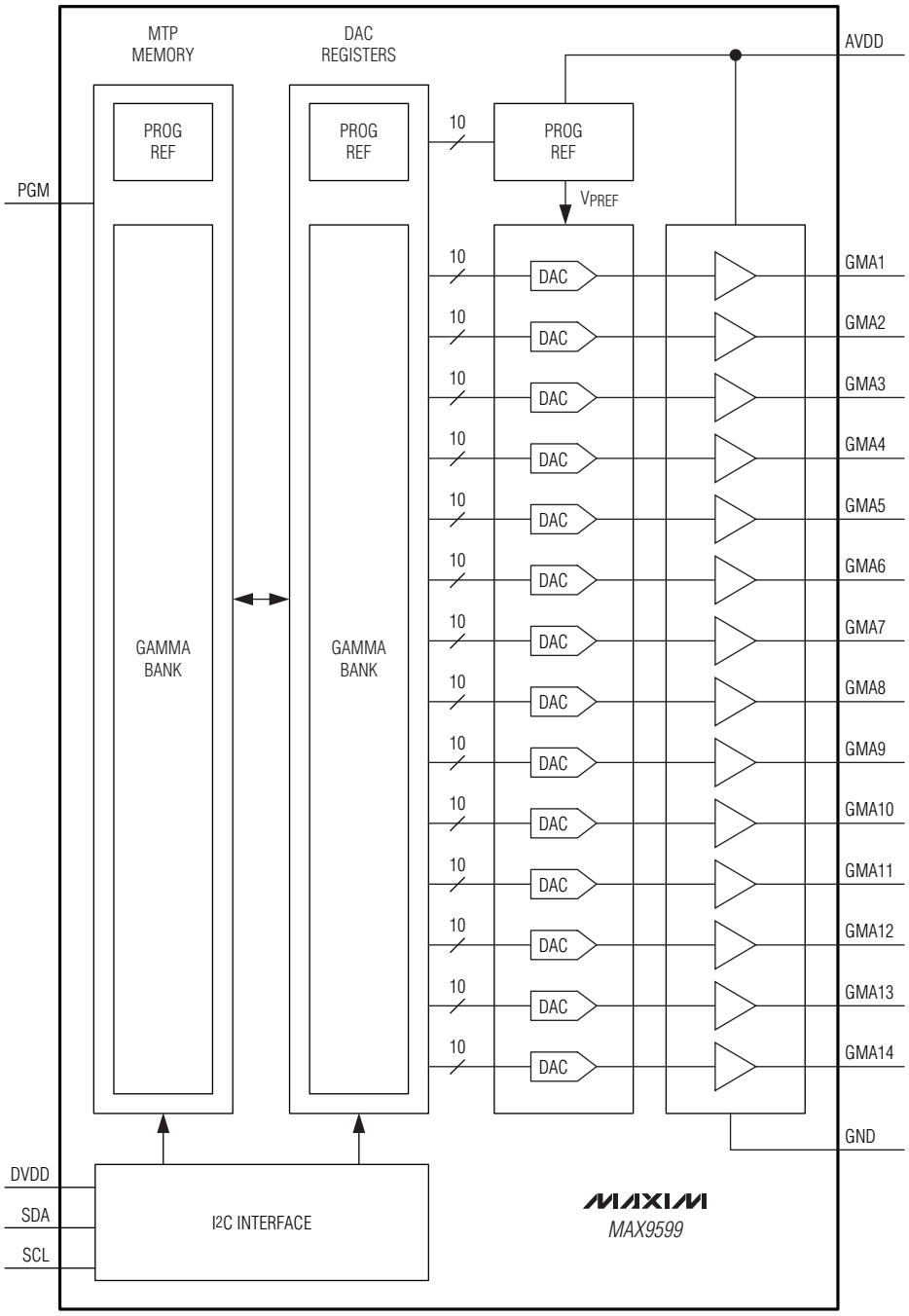


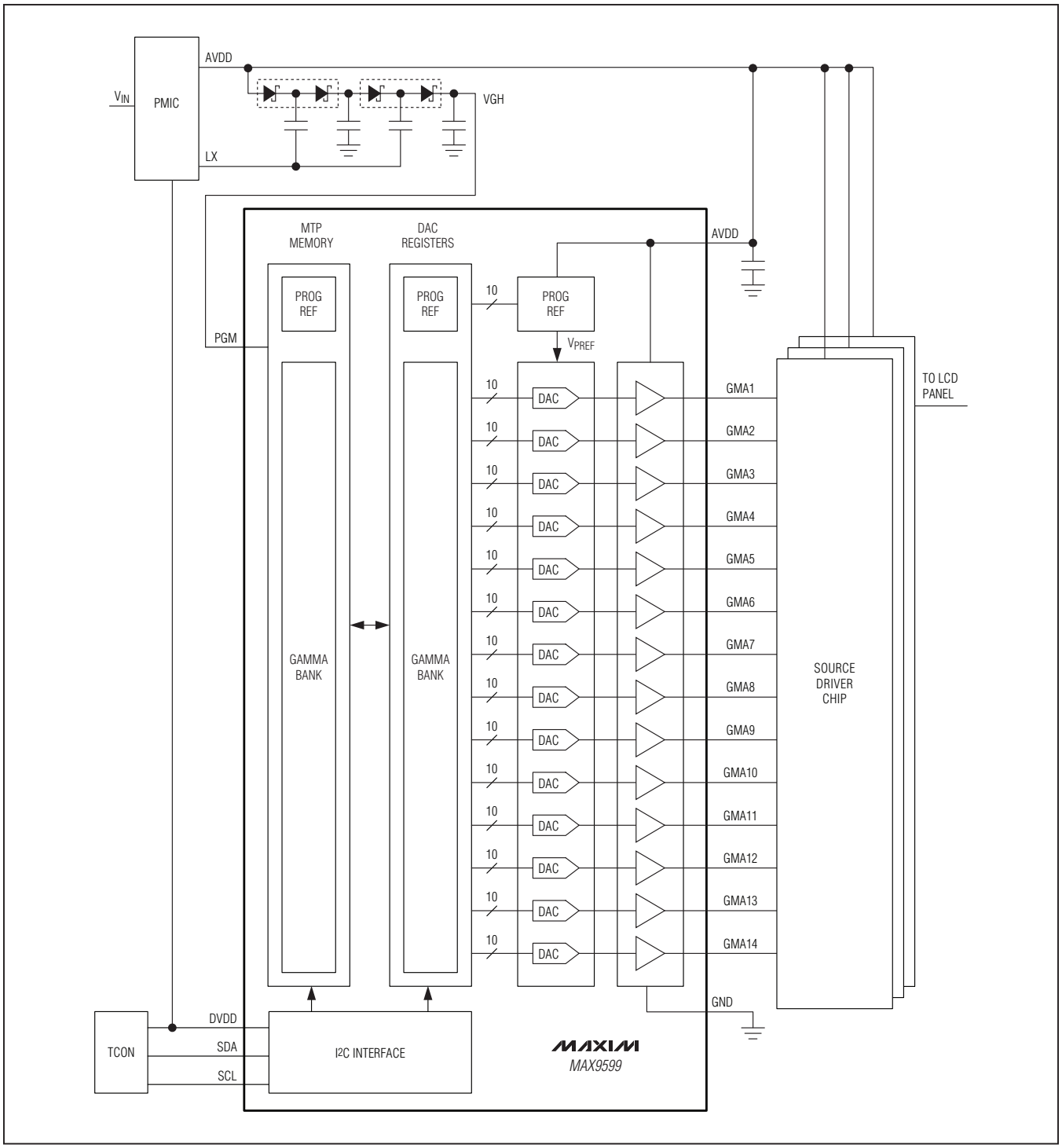
Figure 11. Multiple Small Vias are Recommended over a Single Large Via in the PCB Layout

Functional Diagram



Low-Power Programmable Gamma Buffers

Typical Application Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9599ETG+	-40°C to +85°C	24 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

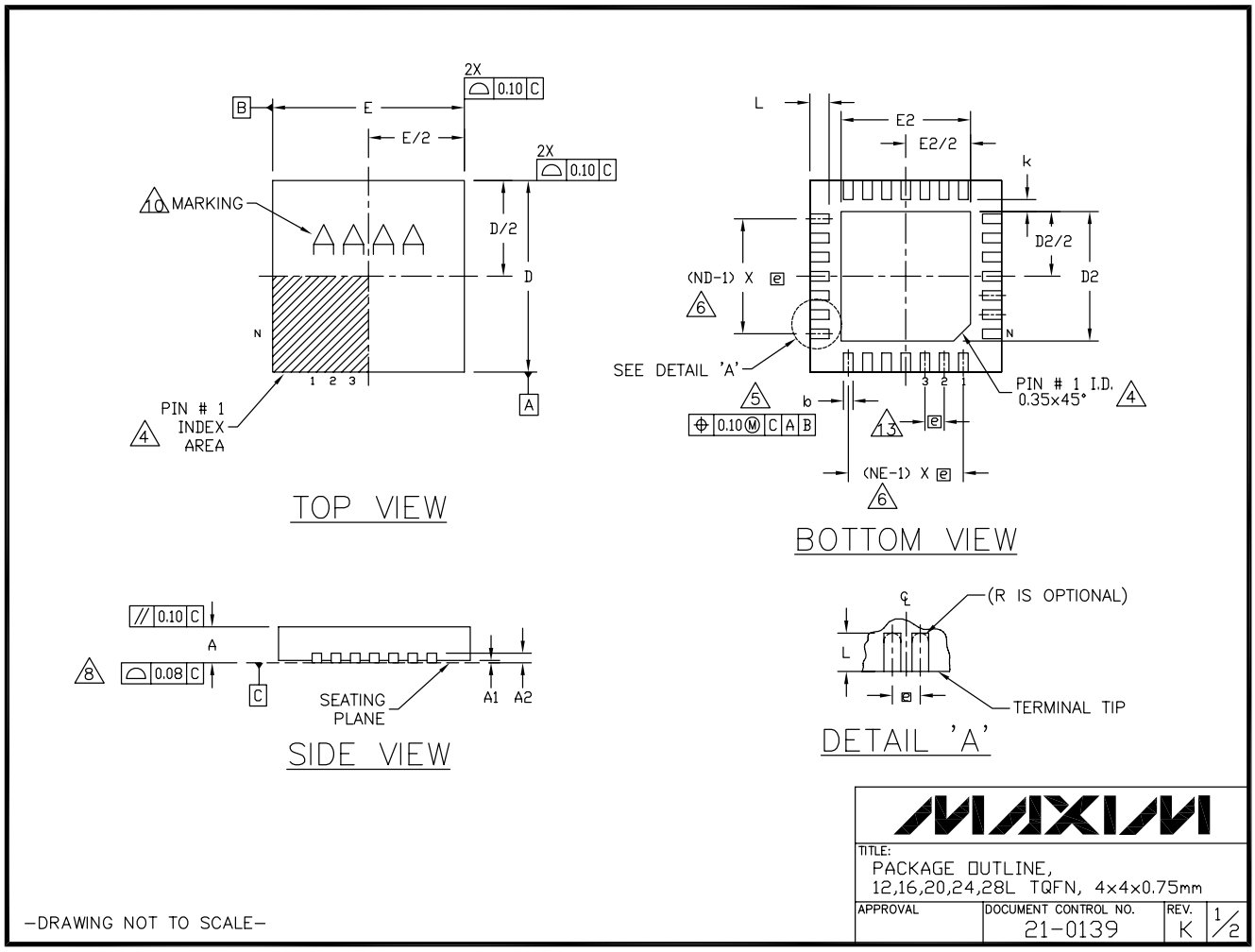
PROCESS: BiCMOS

Low-Power Programmable Gamma Buffers

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 TQFN-EP	T2444+4	21-0139	90-0067



Package Information (continued)

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

COMMON DIMENSIONS

PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63
T2444N-4	2.45	2.60	2.63	2.45	2.60	2.63
T2444M-1	2.45	2.60	2.63	2.45	2.60	2.63
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70
T2844N-1	2.65	2.70	2.75	2.65	2.70	2.75

DIMENSION VARIATIONS

PKG. CODE	D2			E2			L		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T2044-4	2.85	2.90	2.95	2.85	2.90	2.95	0.25	0.30	0.35

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm.
12. WARPAGE SHALL NOT EXCEED 0.10mm.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
15. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC # 10-0131.
16. ALL DIMENSIONS ARE THE SAME FOR LEADED (-) & PbFREE (+) PACKAGE CODES.

–DRAWING NOT TO SCALE–

MAXIM

TITLE:
PACKAGE OUTLINE,
12,16,20,24,28L TQFN, 4x4x0.75mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0139	K	2/2

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/11	Initial release	—